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Conducted EMI Reduction Accomplished via IEEE 1588 PTP for Grid Connected Paralleled Solar Power Inverters

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***Abstract*—This paper introduces a distributed approach for interleaving paralleled power converter to reduce EMI and voltage ripple, accomplished via IEEE 1588 Precision time protocol. An open source software stack of IEEE 1588v2 named PTPd-2.2.0 is used to implement software stack over stellaris series microcontroller from Texas Instruments (TI). A general methodology for achieving distributed interleaving is proposed, along with a specific software based implementation approach using the PTPdv2. The effectiveness of such methods in terms of EMI reduction is experimentally validated in grid connected Paralleled Solar Power Inverters.**

***Index Terms*—IEEE 1588, Precision Time Protocol (PTP), Ethernet networks, time synchronization, Master clock and Slave clock, Electromagnetic Compatibility (EMC), Electromagnetic Interference (EMI), power electronics, power transmission, power converters, ripple cancellation, Micro Controller Unit (MCU)**

I. Introduction

Paralleling of converter power modules is a well-known technique that is often used in high-power applications to achieve the desired output power with smaller size power transformers and inductors. Since magnetics are critical components in power converters because generally they are the size-limiting factors in achieving high-density and low-profile power supplies, the design of magnetics become even more challenging for high power applications that call for high power density and low-profile magnetics. Instead of designing large-size centralized magnetics that handle the complete power, low-power distributed high density low-profile magnetics can be utilized to handle the high power, while only partial power flow through each individual magnetics.

In addition, the switching frequencies of paralleled, low-power processing stages may be higher than the switching frequencies of the corresponding single, high-power processing stages because low-power, faster semiconductor switches like MOSFET, IGBT can be used in implementing the paralleled low-power stages. Consequently, paralleling helps to reduce the size of the magnetic components and to achieve a low-profile design for high power applications.

In its basic form, the interleaving technique [1, 2] can be viewed as a variation of the paralleling technique, where the switching instants of power switches are phase shifted within a fixed switching period. By introducing an equal phase shift of switching instants between the paralleled power stages, the total current ripple of inductor of the power stage seen by the output filter capacitor is lowered due to the ripple cancellation effect. PWM based interleaving technique used in parallel converter system, can reduce output harmonic currents and voltages by phase shifting the real or equivalent carrier waveforms to a certain angle as shown in fig.1. Thus, the interleaving has the potential to reduce the value of AC passive components of paralleled three-phase voltage-source converters (VSCs). However, how to maximize the benefit of interleaving is still not clear without an insightful understanding of the principle of interleaving.

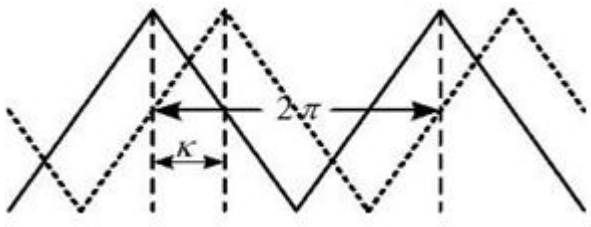

Fig. 1. Definition of interleaving angle (κ)

II. Interleaved Converters

In interleaving technique the switching instants are phase-shifted over a fixed switching period. By providing an equal phase shift between the paralleled power processing stages, the output filter capacitor ripple current is lowered due to the cancellation effect. At the same time, the effective ripple frequencies of the output-filter capacitor current and the input current are increased by the number of interleaved modules. As a result, the size of the capacitance based output filter can be minimized.

Generally, the interleaving in topologies with inductive output filters can be implemented in two ways. First interleaving approach is to directly parallel the outputs of the individual power stages so that they share a common output filter capacitor. The second approach is to parallel the power stages at the input of a common LC output filter. The former approach distributes the transformer and output filter magnetics, while the latter distributes only the transformer magnetics. Due to its distributed magnetics structure and minimum-size output filter, the interleaving technique is

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especially attractive in high-power applications that call for high power-density and low-profile packaging. The active method of interleaving permits to obtain more advantages. In the interleaving method, inverters are operated at the same switching frequency with their switching waveforms displaced in phase over a switching period. The benefits of this technique are due to harmonic cancellation among the inverters, and include low ripple amplitude and high ripple frequency in the aggregate input and output waveforms. It is seen that, interleaved operation of N inverters yields an N-fold increase in fundamental current ripple frequency and a reduction in peak ripple magnitude by a factor of N or more compared to synchronous operation. The advantages of this technique may be summarized in these points:

1. Reduced current ripple and an increased equivalent switching frequency
2. High dynamic performances
3. A possible reduction of switching losses in the conversion action

III. Theoritical Considerations

In modular power supplies with parallel topology, the interleaving technique is used to equally share the total power to be delivered among the number of converters, N [3]. In this case all converters operate with the same frequency but

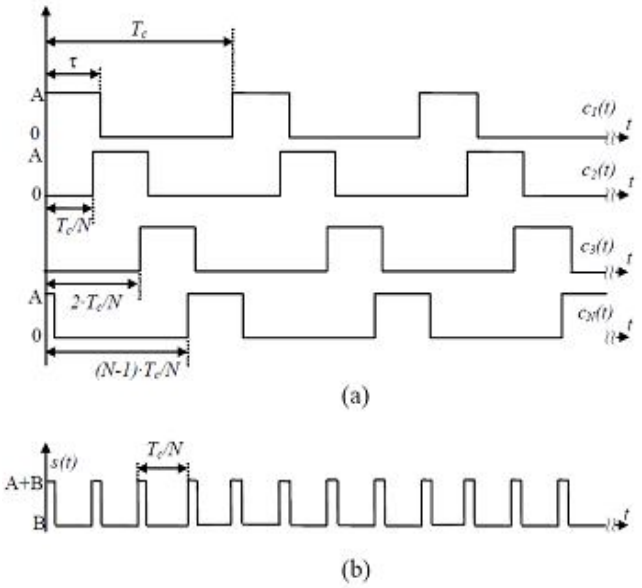

Fig. 2. Interleaving technique for N=4. (a) Switching pattern. (b) Equivalent source of noise pattern

a shift delay equal to T_c/N is introduced in the switching pattern of each converter (Fig. 2a), where T_c is the switching period. From the point of view of the noise generation, the combination of these N switching pattern ($c_i(t)$, with i=1, 2, ...N) results in a signal s(t), which correspond to the equivalent noise generation pattern (Fig. 2b). The expressions in time domain of $c_i(t)$ and the equivalent noise generation pattern, s(t) is given by (1), where sub-index 'i' corresponds to each of the N switching patterns and 'k' notes the switching cycle.

The equivalent noise source pattern generated by all converters is equal to the noise generated by a single converter

$$s(t)=\sum_{i=1}^{N} c_i(t)=A\cdot\left[B+\sum_{k=0}^{\infty}\left(u\left(t-k\frac{T_C}{N}\right)-u\left(t-k\frac{T_C}{N}-\left(\tau-\frac{T_C}{N}\right)\right)\right)\right] \quad (1)$$

where $c_i(t)$ and B are given as:

$$c_i(t)=A\cdot\sum_{k=0}^{\infty}\left(u\left(t-k\frac{T_C}{N}-\frac{T_C}{N}(i-1)\right)-u\left(t-kT_C-\tau-\frac{T_C}{N}(i-1)\right)\right)$$

switching at a constant frequency of $N\cdot f_c$. Whereas in the switching pattern of each individual converter harmonic appears at f_c (Fig. 3a), on the equivalent source of noise pattern they only appear at $N\cdot f_c$ (Fig. 3b). Thus, the interleaving technique has shown itself to be a harmonic cancellation method. The relationship in frequency domain between $C_i(w)$ and S(w) is demonstrated in [4] and is given by (3), where n is the harmonic order and w_c is $2\cdot\pi\cdot f_c$.

$$S(w)=\left|F\left\{\sum_{i=1}^{N} c_i(t)\right\}\right|=\left|C_1(w)\right|\cdot\left|M(w)\right| \quad (2)$$

where M(w) is given as:

$$M(w)=\frac{1-e^{-j\cdot\frac{n\cdot w_C\cdot T_C\cdot N}{N}}}{1-e^{-j\cdot\frac{n\cdot w_C\cdot T_C}{N}}}=\frac{1-e^{-j\cdot 2\cdot\Pi\cdot n}}{1-e^{-j\cdot\frac{2\cdot\Pi\cdot n}{N}}}=\begin{cases}0 & n\neq p\cdot N\\ N & n=p\cdot N\end{cases}\quad p=0,1,2,3..$$

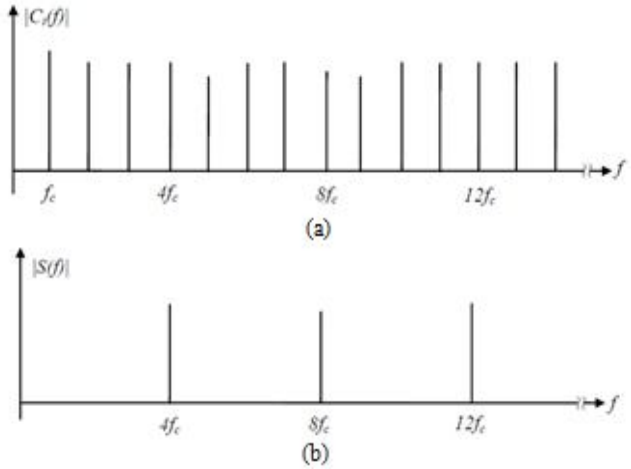

Fig. 3. Harmonics cancellation achieved with interleaving for N=4. (a) Switching pattern spectrum. (b) Equivalent source of noise pattern spectrum

Interleaving N parallel connected inverters requires that the inverters be operated at the same switching frequency but phase displaced with respect to one another by $2\pi/N$ radians. This is achieved by using IEEE 1588 PTP. The precision time protocol (PTP) specified in IEEE 1588 is able to synchronize distributed clocks with an accuracy of less than one microsecond. It is applicable in multicast capable network technologies such as Ethernet LANs. The mechanism combines high accuracy and fast convergence with low demand on clocks and on network and computing capacity.

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IV. A Practical Implementation Method

Time synchronization of distributed computing elements is a common requirement for a number of distributed applications. The IEEE 1588, "Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems" [5, 6] allows timing better than 1μs accuracies for devices connected via a network such as Ethernet.

The IEEE 1588 Precision Time Protocol (PTP) [7-9] provides a means by which networked computer systems can agree on a master clock reference time, and a means by which slave clocks can estimate their offset from master clock time.

There are several timing protocols already available today so why IEEE 1588? This standard has been ratified by the IEEE 1588 and has been designed to overcome the inadequacies of previous solutions such as accuracy, scalability and cost.

However, it is not presently in widespread use because special hardware is required that permits the sending device to know exactly when the message was sent. Knowing accurate timing information permits extremely accurate measurement of network propagation delays that are then used to make precise adjustments to the device clock time. The drawback to this approach, however is that all devices in the network that receive and send messages must have hardware compatible with this standard.

IEEE 1588 (PTP) meets the requirements of providing synchronization for distributed system clocks which are as follows:

- High precision (< μ s).
- Applicable in any multicast network,
- Support of a heterogeneous mix of distinct clocks with different characteristics (accuracy, resolution, drift, stability).
- Administration-free, simple installation.
- Easy configuration
- Fast convergence.
- Moderate demand for channel bandwidth and computing resources.

V. Ptp In Brief

In PTP, master clocks provide the reference time for one or more slave clocks through the exchange of messages over a network. The protocol determines a unique master among a group of clocks using the Best Master Clock algorithm (BMC). Basic PTP scheme of synchronization network is given at fig. 4. IEEE 1588 is a standard that specifies a protocol to synchronize independent clocks running on separate nodes of a distributed relatively localized network. The clocks communicate with each other through a bidirectional multicast communication and four 1588 messages are necessary for the synchronization process: Sync, Follow_up, Delay_Req and Delay_Resp. The messaging between the master and the slave clocks is depicted in fig. 5.

For a slave node to synchronize with a master node, two

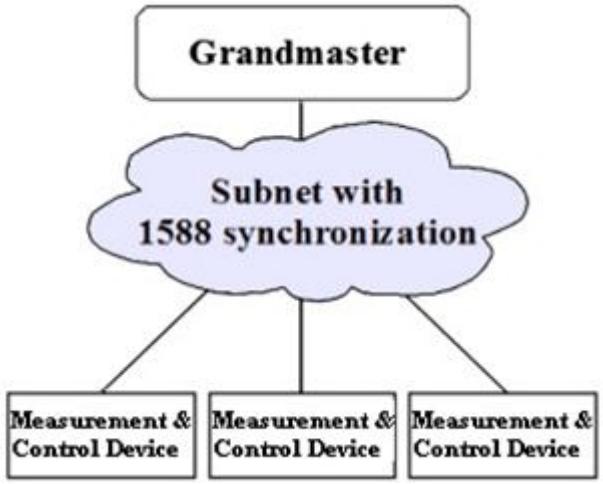

Fig.4. Scheme of Synchronization network

quantities must be determined: the slave node's clock offset in relation to the master's clock (offset) and the network propagation delay (d_{prop}). Considering that the master-to-slave delay is equal to the slave-to-master delay and by using the four messages illustrated in fig. 5, these quantities can be calculated from the four measured unique values t1, t2, t3 and t4.

The master sends a Sync message to the slave and notes the time, t1, at which it was sent. The slave receives the Sync message and notes the time of reception, t2. The master conveys to the slave the timestamp t1 by either

- Embedding the timestamp t1 in the Sync message (one-step) or
- Embedding the timestamp t1 in a Follow-Up message (two-step).

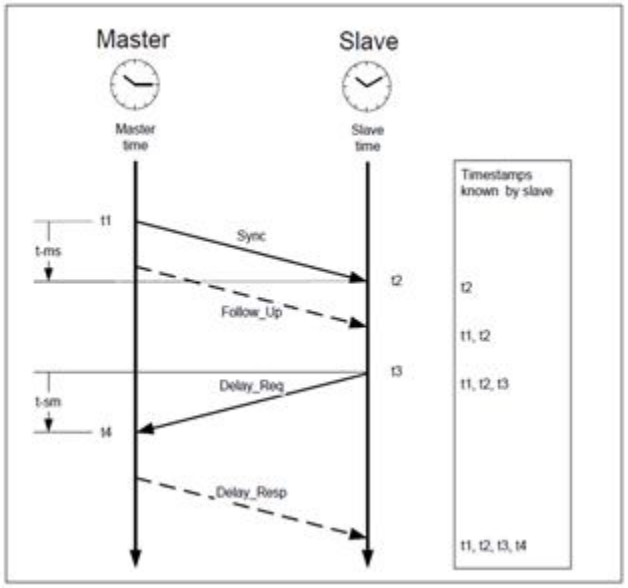

Fig. 5. Synchronization timing diagram

The slave sends a Delay_Req message to the master and notes the time, t3, at which it was sent. The master receives the Delay_Req message and notes the time of reception, t4. The master conveys to the slave the timestamp t4 by embedding it in a Delay_Resp message.

The difference between the send and receipt times of Sync

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messages is the master-to-slave delay (t_{ms}). The difference between the send and receipt times of Delay Request messages is the slave-to-master delay (t_{sm}).

$$t_{ms} = t1 - t2 \quad (5)$$

$$t_{sm} = t3 - t4. \quad (6)$$

A. One way delay

PTP calculates an estimate of the message propagation delay. This calculation assumes symmetric propagation delays, so that an average of the master-to-slave and slave-to-master delays cancels the time offset between master and slave. This yields the message propagation delay, which the specification refers to as the one-way delay (d_{prop}):

$$d_{prop} = \frac{t_{ms} + t_{sm}}{2} \quad (7)$$

The slave averages the both directional delays and then adjusts the clock by the time of the delay in order to synchronize the two clocks.

B. Offset from Master

PTP estimates the time difference between master and slave clocks. The master-to-slave delay corrected for message propagation delay, and it is referred to as the offset from master (Δt):

$$\Delta t = t_{ms} - d_{prop} \quad (8)$$

Since the master and slave clocks drift independently therefore, periodic offset and delay correction is necessary to maintain clock synchronization.

VI. PTP And Distributed Interleaving Approach

In an AC Power system, the generator or, in our case, the solar inverter, carrier PWM technique is used to control switching operation of power electronics inverter (DC to AC). Carrier shifting PWM Technique is used for to implement interleaves technique in distributed parallel inverters to reduce conducted EMI. This, however, is possible only if the MCUs in question have a common or synchronized system clocks, so that their functions can be perfectly coordinated. This can be achieved by using the Precision Time Protocol, standardized as IEEE 1588. The digital high-precision 1 PPS (pulse per second) signal is used as reference signal for time and phase synchronization purpose. The signal is a simple rectangular 1 Hz pulse, whose rising or falling edge marks the start of a new second. The synchronization accuracy of the rectangular pulse signal is in the range of a few nano seconds.

The inverter in question is an H-type full bridge DC/AC Inverter, controlled by a MCU as shown in fig 6. An H-Bridge or full bridge converter is a switching configuration composed of four switches in an arrangement that resembles an H. By controlling different power switches in the bridge, a positive, negative, or zero potential voltage can be placed across a load. This, in combination with an LC filter, is used to generate a sine wave from a dc signal. The switches of the

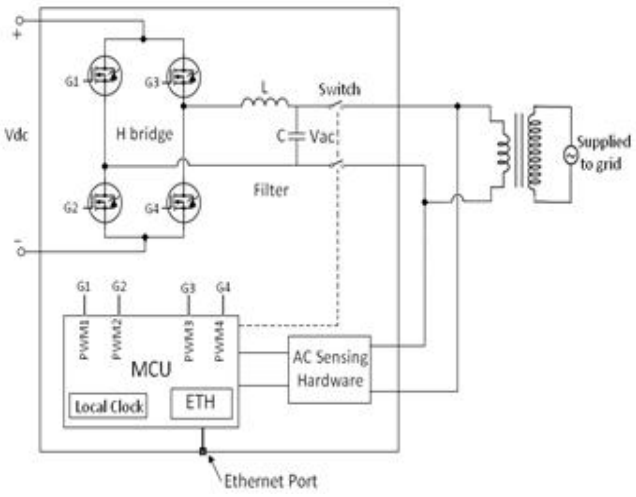

Fig. 6. Inverter's internal diagram

H-Bridge configuration are implemented using MOSFET. The MOSFET switches are driven by PWM signals from the MCU. To achieve distributed interleaving, all of the inverters are connected by an Ethernet network, typically consisting of Ethernet cables, Ethernet socket, Router, Switches, hub etc as shown in fig 7 and 8. Each inverter has its own clock generator, and places information about the frequency and phase of its local clock on the Ethernet network. Using the aggregated information on the Ethernet network, each inverter adjusts the frequency and phase of its own clock source to achieve the desired interleaved effect.

In the new distributed interleaving approach, the Ethernet network needed to attain interleaved operation is distributed among the Inverters, with only minimal connections among Inverters. The connections among Inverters are noncritical,

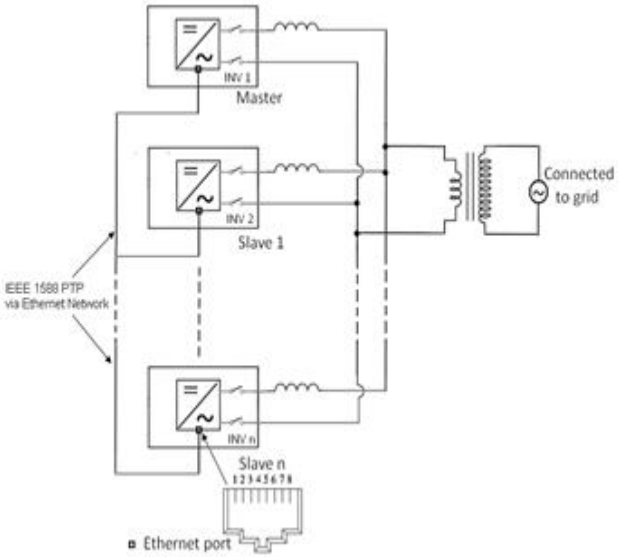

Fig. 7. General topology of distributed inverters

i.e., failure of the connection disrupts only the interleaving function, not the basic operation of the system. The approach automatically accommodates varying numbers of inverters. If an individual inverter is removed or fails, the remaining inverters automatically interleave among themselves. Any failures affecting the information-sharing connections inhibit

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the interleaving, but do not cause the system to fail. These attributes lead to a flexible, reliable, and robust interleaving system.

The results are displayed in fig. 9 and 10. Master and Slave electric drive system clocks are synchronized with the accuracy of approximately in range 40-50µs using PTP software only implementation. If precision time protocol is processed using hardware assisted time stamping then accuracy of clocks synchronization is in 10-20 ns range. Using synchronized clock of parallel distributed Inverter we can synchronized Carrier signal, required to control switching operation of power electronics converters. Now, for interleaved operation required to phase shift of salves carrier signals with respect to master's carrier signal, it is dependent on number of parallel connected inverters. It is possible sharing information about carrier signal phase using Ethernet communication in between master & slaves inverters. Slaves adjust phase of carrier signal as per information sharing with master. Therefore, as per interleaving technique conducted

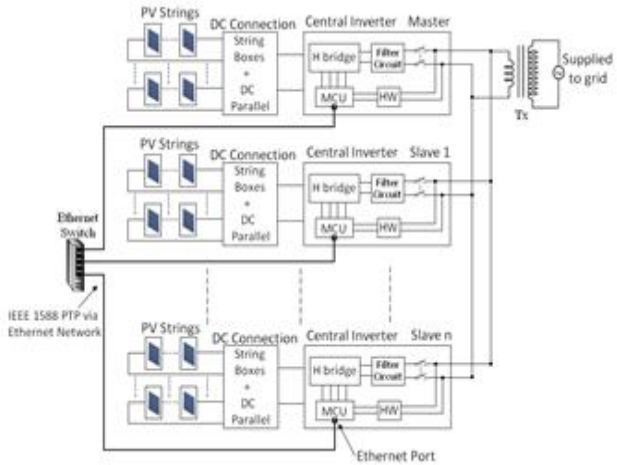

Fig. 8. Carrier synchronization of Solar inverters with IEEE 1588 via Ethernet networks

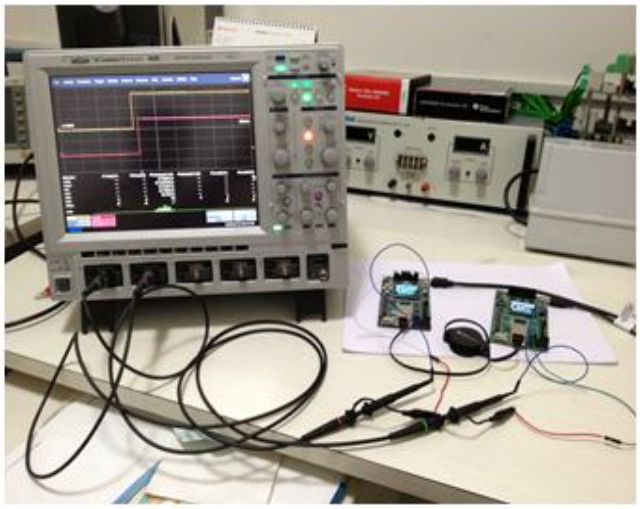

Fig. 9. Experimental Setup

EMI are cancel out to each other and result into highly accurate output with reduced conducted EMI as shown in fig 11 and 12. Also we can share events & information with precise & accurate time stamping between Parallel connected Drives using PTP if necessary for controlling & measurement operation of parallel Inverters. Thus two very important benefits of PTP are mentioned above in parallel inverters operation.

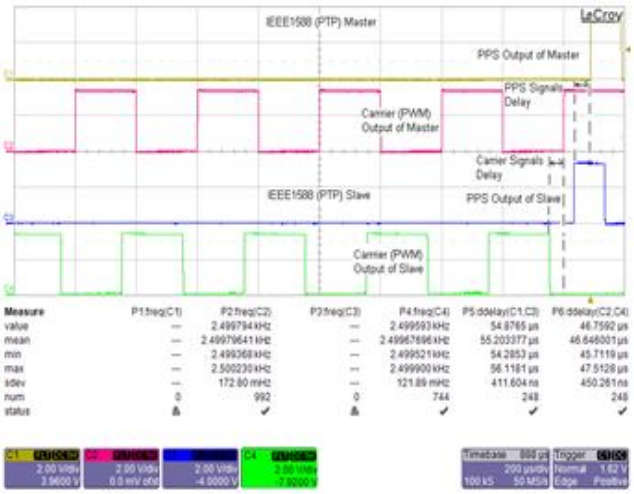

Fig. 10. Synchronized PPS signals and Carrier PWM Signals

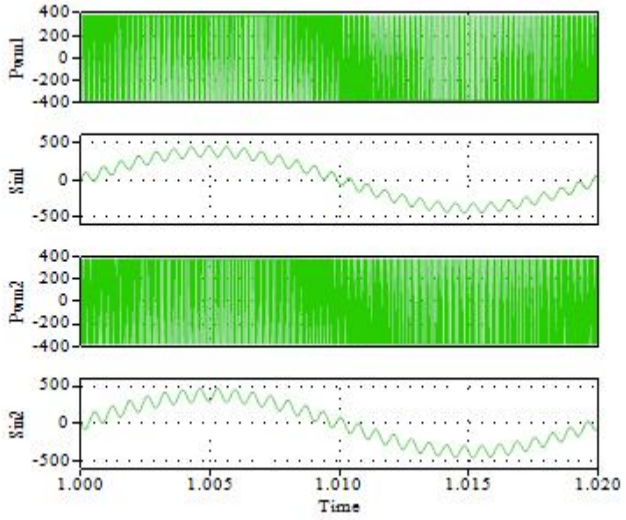

Fig. 11. Simulation results without interleaving

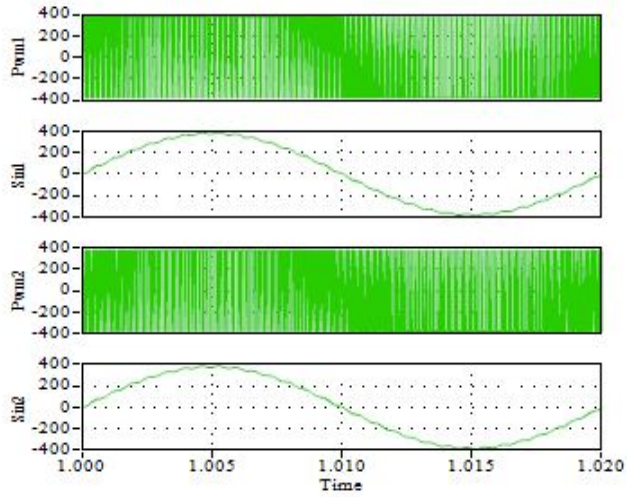

Fig. 12. Simulation results with interleaving of two inverters

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Conclusions

The paper has introduced a distributed approach to interleaving converter in which the Ethernet based IEEE 1588 PTP protocol stack is used to attain interleaving among the parallel converters. The protocol IEEE 1588 could be implemented in two different approaches: software-only or hardware-assist. In software only implementation, the protocol is wholly executed at the application level and the accuracy will depend mainly on software and how the hardware layer executes the firmware source code. Hardware-assisted implementation delivers more precise time synchronization. Proposed system is implemented using stellaris series microcontroller from Texas Instrument which also includes hardware-assisted support for synchronization using the IEEE 1588 Precision Time Protocol. An open source stack of IEEE 1588v2 named PTPd-2.2.0 is used to implement software. The experimental results corroborate the analytical predictions and demonstrate the tremendous benefits of the distributed interleaving approach via IEEE 1588.

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Biographies

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Venu Uppuluri Srinivasa holds Master's degree in Mechanical from Osmania University, Hyderabad, A.P, India. Has over 20 years of experience as an IT / ITes Technologist with both established public companies and Venture funded startups. Currently working as General Manager and Head for Carraro Technologies India Limited since 6 years representing Board as an authorized signatory. Also signed as board of director for Santerno India Private Limited. Served in the capacity of Engineering Director for Emerson Electric Co. (USA), Group Manager for Tecumseh Products India Limited etc.

Mangesh Kadam received the B.E. degree in E&TC engineering from Pune University, MH, India, in 2008. From 2009 to 2011, he was with the Research Center, Electronet Equipment, Pune, India, where he was working on development of Automation & Automotive products like process control & measurement equipments, Data Logger, Throttle Paddle controller. Since July 2011, he has been with the Santerno India Design Center, Pune, India. His research interest includes Embedded System Design, Control system Design, Linux & Embedded Linux, RTOS, Device Driver & Communication protocols development.

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